APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,671	01/17/2002	Amr M. Mohsen	003921.00248	6141

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BANNER & WITCOFF, LTD.
1100 13th STREET, N.W.
SUITE 1200
WASHINGTON, DC 20005-4051

EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED <u>13 November 2007</u> FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

   a) ☒ The period for reply expires <u>3</u> months from the mailing date of the final rejection.

   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

      Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

<u>NOTICE OF APPEAL</u>

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

<u>AMENDMENTS</u>

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will <u>not</u> be entered because

   (a)☐ They raise new issues that would require further consideration and/or search (see NOTE below);

   (b)☐ They raise the issue of new matter (see NOTE below);

   (c)☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d)☐ They present additional claims without canceling a corresponding number of finally rejected claims.

      NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

<u>AFFIDAVIT OR OTHER EVIDENCE</u>

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will <u>not</u> be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will <u>not</u> be entered because the affidavit or other evidence failed to overcome <u>all</u> rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

<u>REQUEST FOR RECONSIDERATION/OTHER</u>

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
   <u>See Continuation Sheet.</u>

12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

Continuation of 11. does NOT place the application in condition for allowance because:

Applicant's remarks are not persuasive.

The "arguments from April 6, 2007" have been addressed in an earlier office action.

The IBM document discloses interconnected programmable chips on a substrate which are connnected to and configured by another chip or part of a chip. With respect to claims disclosing multiple layers of conductive traces, see pp. 296-297 and fig. 6. With respect to claim limitations concerning discrete elements, see # 5 of page 298.

Note that each chip site is surrounded by a switch bed.

Carter discloses reconfigurable logic. See figure 4a. FIGS. 4A illustrates a configurable logic array containing nine configurable logical elements. As shown in FIG. 4A, each CLE of the nine CLEs 40-1 through 40-9 has a plurality of input leads and one or more output leads. Each input lead has a plurality of access junctions each connecting a selected general interconnect lead to the input lead. The access junctions for input lead 2 of CLE 40-7 are labeled A1 through A4 in FIG. 4A. The access junctions for the other input leads are indicated schematically but are not labeled for the sake of clarity. Similarly, each output lead of each CLE has a plurality of access junctions each connecting the output lead to a corresponding one of the general interconnect leads.

Applicant's argument/distinction regarding Carter is not understood.

It appears a "standard configuration" consitutes known (standard) practices in the art. Regardless, even if Applicant's arguments were accurate, the ability to provide for a "personalization of the interconnection" is not a "teaching away" from a "standard configuration". Instead, this refers to the ability to modify a "standard configuration". In any case, applicants have provided no evidence that there is a functional distinction between a "standard" and a "personalized" configuration. Furthermore, what if the personalized configuration was, in fact, chosen to be a "standard configuration"? How would one looking at a configuration know whether it was standard or personalized?

Applicant also appears to argue that the leads must be separate from any PIC in the IBM teaching. It is recognized that merely making separable is not sufficient to distinguish over the prior art, In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961). It is also recognized that merely making integral is not sufficient to distinguish over the prior art, In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) Regardless, it is not clear how the PIC in the IBM teaching would function without a direct connection. It is noted that the disclosed circuits can function even when some of the chips are removed and furthermore that removing the chips does not alter any of the mechanical parts in the circuit.